

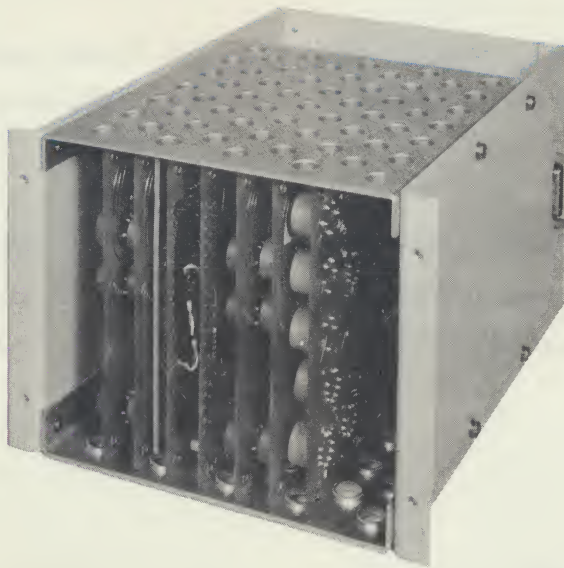
COMMUNICATION BUFFER

Magnetic Core Delay Line

ENGINEERING DATA SHEET


DI/AN CONTROLS INC.

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$$\text{MCDL} - \begin{bmatrix} \text{S/S} \\ \text{S/P} \\ \text{P/S} \\ \text{P/P} \end{bmatrix} - 50$$

GENERAL DESCRIPTION

The DI/AN "MDCL" series Communication buffer is the lowest priced Sequential Access Buffer available today. Designed as a Magnetic Core Delay Line, the "MDCL" series features digital magnetic circuitry and modular construction throughout. An "off-the-shelf" system, this buffer meets applications previously filled by more expensive and less reliable multiple delay line equipments presently on the market, while providing functional advantages inherent only in magnetic core memory systems.

The basic MCDL-S/S-50 Communication Buffer contains a core array of up to 1386 bits which is selected on four coordinates by mutually prime ring counters. Each ring counter stage employs a standard DI/AN digital magnetic Core-Transistor Drive Module and, as such, provides both the shift and core drive function in each circuit.

The parallel data output feature of the MCDL-S/P-50 model is obtained by adding an economical Magnetic Core Rope Card to the basic MCDL-S/S-50 unit which will accommodate up to 16 parallel output bits.

Further system flexibility is achieved by adding a standard DI/AN digital magnetic Shift Register Card providing up to 12 parallel input data channels. This latter model is designated MCDL-P/P-50.

By making the "MCDL" series available in a selected number of storage capacities and utilizing a minimum variety of component types, the attendant advantages of large quantity component purchases coupled with volume production has resulted in a remarkably low unit-price.

FEATURES

- Non-volatile Storage of Data
- Low Standby Power
- Data Format Flexibility
- High Noise Immunity
- All Silicon Circuitry
- High Storage Density
- Modular Construction

FOUR MODELS AVAILABLE

MCDL-S/S-50	Bit Serial In; Bit Serial Out
MCDL-S/P-50	Bit Serial In; Bit Parallel Out
MCDL-P/S-50	Character Parallel In; Bit Serial Out
MCDL-P/P-50	Character Parallel In; Character Parallel Out

APPLICATIONS

Communications Terminal Buffer

Transmission	MCDL-P/S-50
Receiver	MCDL-S/P-50

Data Formatting

Serial-Parallel	MCDL-S/P-50
Parallel-Serial	MCDL-P/S-50
n Parallel	MCDL-P/P-50
m Parallel	

Block or Line Buffer

MCDL-S/S-50

I/O Buffer

MCDL-P/P-50

Event Indexing

MCDL-S/S-50

Telemetry Buffer

MCDL-S/P-50

MCDL-P/S-50

OPERATING CHARACTERISTICS

Bit Rate	0 to 5×10^4 Bits/Sec (asynchronous)
Storage Capacity	Up to 1386 Bits
Operating Modes	Read/Restore Clear/Write
Input Data	Bit Serial or up to 12 Parallel Bits
Output Data	Bit Serial or up to 16 Parallel Bits

ELECTRICAL SPECIFICATIONS

	<u>Voltage</u>	<u>Current</u>	<u>Width</u>
Initiate Pulse	-6v	50 ma (sink)	3.0 usec
R/R Mode	-6v	5 ma (sink)	Full cycle level
C/W Mode	-6v	5 ma (sink)	Full cycle level
Data In			
"1"	0v	<0.5 ma	10 usec (serial) 4 usec (parallel)
"0"	-6v	30 ma	10 usec (serial) 4 usec (parallel)
Data Out*			
"1"	0v	10 ma (source)	2 usec
"0"	-6v	<0.5 ma	Level
Operating Power**	+6v	250 ma	--
	-6v	800 ma	--
Standby Power	+6v	50 ma	--
	-6v	200 ma	--

* 0 and +6 interface voltage levels are also available.

** at 5×10^4 Bits/Sec for 1386 bit capacity.

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature Range	+10 to +40°C
Storage Temperature Range	-20 to +80°C
Relative Humidity	up to 90%
Shock and Vibration	as normally encountered in shipping and handling.

PHYSICAL SPECIFICATIONS

Height	5-3/8 inches
Width	6-1/2 inches
Depth	7-1/2 inches
Weight	5-1/2 lbs.